CLAIMS:

1. Integrated circuit (1) comprising:

- an electric device (2) comprising a first silicon layer (120) having a silicidated part (122) and a non-silicidated part (123), and
- a further electric device (3), the further electric device comprising a dielectric layer (130) having a dielectric layer thickness (D),

wherein the non-silicidated part (123) of the electric device is covered by a further dielectric layer (131) having the dielectric layer thickness (D), the silicidated part (122) not being covered by the further dielectric layer (131).

2. Integrated circuit (1) as claimed in claim 1, wherein the electric device (2) comprises a resistor.

3. Integrated circuit (1) as claimed in claim 2, wherein the silicidated part (122) of the resistor comprises a first contact area (128) and a second contact area (129), the non-silicidated part (123) separating the first contact area (128) from the second contact area (129).

4. Integrated circuit (1) as claimed in claim 1, wherein the dielectric layer (130) of the further electric device (3) is at least partly covered by a second silicon layer (140) having a second silicon layer thickness (S'), the further dielectric layer (131) of the electric device (2) being at least partly covered by a third silicon layer (141) having the second silicon layer thickness (S').

5. Integrated circuit (1) as claimed in claim 4, wherein the second silicon layer (140) and the third silicon layer (141) are silicidated.

6. Integrated circuit (1) as claimed in claim 4, wherein the third silicon layer (141) has a sidewall being provided with an insulating sidewall spacer (16).

7. Integrated circuit (1) as claimed in claim 4, wherein the further electric device (3) comprises a capacitor having a capacitor dielectric layer and a capacitor electrode layer, the dielectric layer (130) comprising the capacitor dielectric layer, the second silicon layer (140) comprising the capacitor electrode layer.

8. Integrated circuit (1) as claimed in claim 4, wherein the further electric device (3) comprises a field effect transistor having a gate dielectric layer and a gate electrode layer, the dielectric layer (130) comprising the gate dielectric layer, the second silicon layer (140) comprising the gate electrode layer.

9. Integrated circuit (1) as claimed in claim 4, wherein the further electric device (3) comprises a non-volatile memory cell having a gate stack comprising a floating gate layer (121), an intergate dielectric layer and a control gate layer, the floating gate layer (121) being composed of silicon and having a thickness (S) which is identical to that of the first silicon layer (120), the dielectric layer (130) comprising the intergate dielectric layer, the second silicon layer (140) comprising the control gate layer.

10. Integrated circuit (1) as claimed in claim 4, wherein the further electric device (3) comprises a bipolar transistor having a base region (150) and an emitter layer contacting the base region (150) in an emitter-base contact area (151), a part of the emitter layer comprising the emitter-base contact area (151) being delimited by an opening in the dielectric layer (130), the emitter layer being constituted by the second silicon layer (140).

11. A method of manufacturing an integrated circuit (1) as claimed in claim 1, the method comprising the steps of:

providing a prefabricated integrated circuit having the first silicon layer (120),

providing a layer (13) of a dielectric material having the dielectric layer thickness (D),

patterning the layer (13) of the dielectric material to simultaneously form the dielectric layer (130) and the further dielectric layer (131), and

forming the silicidated part (122).

12. A method as claimed in claim 11, wherein the dielectric layer (130) of the further electric device (3) is at least partly covered by a second silicon layer (140) having a

second silicon layer thickness (S'), the further dielectric layer (131) of the electric device (2) being at least partly covered by a third silicon layer (141) having the second silicon layer thickness (S'), the method further comprising the steps of:

providing a layer (14) of silicon having the second silicon layer thickness (S'), and

patterning the layer (14) of silicon to simultaneously form the second silicon layer (140) and the third silicon layer (141).

13. A method as claimed in claim 12, wherein the third silicon layer (141) has a sidewall being provided with an insulating sidewall spacer (16), the method further comprising the step of providing the sidewall spacers (16).